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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,491	01/05/2006	Francois Vacherand	126394	8282

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EXAMINER	
YU, HENRY W	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
12/18/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/563,491	VACHERAND ET AL.	
	Examiner	Art Unit	
	HENRY YU	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to applicant's communication filed on October 14, 2009, in response to PTO Office Action mailed on August 13, 2009. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, **claim 18** has been amended. As a result, **claims 18-27** are now pending in this application.

Response to Arguments

3. Applicant's arguments filed on October 14, 2009, in response to PTO Office Action mailed on August 13, 2009, have been fully considered and are persuasive. Hence, the rejection has been withdrawn. However, upon further review a new ground of rejection has been made in view of Sotek et al. (Patent Number US 6,209,022 B1).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 18-22 and 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner et al. (Patent Number US 3,737,858) in view of Olarig (Patent

Number US 6,175,889 B1) and in further view of Sotek et al. (Patent Number US 6,209,022 B1).

As per **claim 18**, Turner et al. discloses "*method of addressing an array of microsystems* ***(multiple remote transponders)*** *which can be individually addressed by a control circuit* ***(telemetering system includes a central station)****, the control circuit and each microsystem including an electromagnetic transmission means* ***(though Turner et al. prefers the use of coaxial cables, the transmission medium may also include radio links; Column 4, lines 36-46)****, and each microsystem further including a counter* ***(each transponder includes a counter for counting interrogate pulses; Column 5, lines 47-48)****… and a read-only memory containing a unique identification code* ***(each transponder has a decoding circuit (emphasis), which responds only when the interrogate pulse count is equal to a number assigned to one of its transducers (Column 5, lines 46-55), indicating that the transponder and corresponding transducer store the expected number of pulses in order to make a proper comparison. The system also discloses the use of memory to store transducer states (Column 6, lines 16-19), which can easily be utilized within transponders and corresponding transducers)****,*" and "*an addressing phase, where the control circuit transmits successive increment signals simultaneously to all the microsystems* ***(the control logic circuit 13 counts interrogate pulses; Column 5, lines 24-25)****, and where the microsystems control resetting of their respective counters and, upon receipt of an increment signal, the microsystems increment a content of their respective counters* ***(each transponder includes a counter for counting interrogate***

pulses (Column 5, lines 47-48), with the counter being recycled at the completion of each interrogate cycle; Column 6, lines 24-26) *and compare the content and their respective reduced addressing code, so as to trigger execution of a pre-determined command when the content of the counter and the reduced addressing code are identical* ***(each transponder also contains a decoding circuit (emphasis) which initiates generation of a reply pulse when the interrogate pulse count is equal to a number assigned to one of its transducers; Column 5, lines 46-55)***." Though Turner et al. discloses "*where the control circuit successively addresses each microsystem by its respective identification code* ***(Column 5, lines 46-55)***," Turner et al. does not explicitly disclose "*a register*" or "*the method comprising: an initialization phase...and stores a unique corresponding reduced addressing code in the respective registers of the microsystems*." Turner et al. also does not explicitly disclose "*wherein the unique identification code of each microsystem is different from the unique identification code of each other microsystem, and the unique corresponding reduced addressing code of each microsystem is different from the unique corresponding reduced addressing code of each other microsystem*."

Olarig discloses "*a register* ***(configuration registers; Column 11, lines 52-53)***" and the idea where addressing data is stored in registers during initialization as "*the method comprising: an initialization phase…and stores a unique corresponding reduced addressing code in the respective registers of the microsystems* ***(memory and I/O address ranges are stored in the device's configuration registers during initialized at startup (POST); Column 11, lines 50-56)***."

Sotek et al. discloses the idea of utilizing unique identification codes as "*wherein the unique identification code of each microsystem is different from the unique identification code of each other microsystem* ***(since all the identification codes ID are to be different; Column 5, lines 61-67)***," which also applies to "*the unique corresponding reduced addressing code of each microsystem is different from the unique corresponding reduced addressing code of each other microsystem* ***(Column 5, lines 61-67)****, and for each microsystem, the number of bits representing the unique identification code is greater than the number of bits representing the reduced addressing code* ***(the slave station S can be assigned a new address which has substantially fewer bits than its identification code ID; Column 5, lines 56-59)***."

Turner et al., Olarig, and Sotek et al. are analogous art in that they both have means of addressing a device/unit.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by Turner et al. to also include a process of storing address data during initialization as disclosed by Olarig, which notes the flexibility of configuring registers within the peripheral devices (for example memory space allocation and interrupt priorities), which is especially prevalent in the area of "plug and play" **[Column 3, lines 26-36]**.

As for Sotek et al., the advantage of a smaller number of address bits is that the addressing procedures can be substantially shortened **[Column 6, lines 3-10]**.

As per **claim 19**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses

"*the respective reduced addressing code of a microsystem is a function of its position in the array* ***(the transponders are arranged in channels, with the transponders in each channel designated by the channel designation (this passage indicates different channel ID values) followed by a letter designation; Column 5, lines 38-42)***."

As per **claim 20**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses "*the reduced addressing codes of the microsystems correspond to increasing numbers* ***(the channel designations are sequential from I, II – M. The same sequential increase also applies to the letter designation, which goes from A, B – m; Column 5, lines 38-42)***."

As per **claim 21**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses "*the microsystems are arranged in lines* ***(channels with designations I, II - M)*** *and columns* ***(letter designations with A, B – m; Column 5, lines 38-42)****, the respective reduced addressing code of each microsystem comprising a line number and a column number respectively stored in line and column registers of the microsystems* ***(each transponder, with its corresponding transducer, is assigned a number pertaining to channel and letter designation. An example used is IA (channel I, letter A); Column 5, lines 51-55)****, the contents of line and column registers being respectively compared with the contents of the line and column counters of the microsystem* ***(each transponder includes a counter for counting interrogate pulses and a decoding***

circuit (emphasis) which initiates generation of a reply pulse when the interrogate pulse count is equal to a number assigned to one of its transducers; Column 5, lines 46-55)."

As per **claim 22**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses "*the control circuit successively transmits line increment signals and column increment signals* ***(the control logic circuit 13 counts interrogate pulses; Column 5, lines 24-25)****, the line increment signals causing the contents of the line counters to be incremented and the column increment signals causing the contents of the column counters to be incremented* ***(it should be noted the channel designations are sequential from I, II – M. The same sequential increase also applies to the letter designation, which goes from A, B – m; Column 5, lines 38-42)*** *and the line counters to be reset* ***(the interrogate pulse counters in control logic circuit 13 and in the transponders are recycled at the completion of each interrogate cycle; Column 6, lines 23-26)***."

As per **claim 25**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses "*a microsystem transmits an acquit signal after the execution of the command by the microsystem* ***(after receiving the interrogate pulses from the transmitter/receiver 12, the transponder sends back a replay frequency (Column 10, lines 20-21) to the central station indicating a particular state value; Column 6, lines 35-43)***."

As per **claim 26**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses "*the control circuit* ***(the control logic circuit 13)*** *transmits data representative of a type of command to be executed by the microsystems in association with transmission of a reset signal* ***(after each interrogate cycle, the counters of the control logic circuit 13 and transponders are recycled (reset) (Column 6, lines 23-26), which indicates that another interrogate cycle is to be done)***."

As per **claim 27**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Turner et al. further discloses "*the control circuit* ***(the control logic circuit 13)*** *transmits data representative of a type of command to be executed by the microsystems in association with transmission of an increment signal* ***(the control logic counts interrogate pulses (Column 5, lines 24-25) directed at a particular transponder with its corresponding transducer, which causes the particular transponder with its corresponding transducer to send a reply pulse back to central station; Column 6, lines 10-16)***."

6. **Claims 23-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner et al. (Patent Number US 3,737,858), Olarig (Patent Number US 6,175,889 B1), and Sotek et al. (Patent Number US 6,209,022 B1) in view of Comiskey et al. (Publication No. US 2002/0063661 A1).

As per **claim 23**, the combination of Turner et al., Olarig, and Sotek et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Though Turner et al. discloses "*the microsystems are arranged in lines* ***(channels with designations I, II -***

M), in columns ***(letter designations with A, B – m; Column 5, lines 38-42)***" as well as "*stored in an additional register* ***(each transponder, with its corresponding transducer, is assigned a number pertaining to channel and letter designation. An example used is IA (channel I, letter A); Column 5, lines 51-55)****...each microsystem comprising an additional counter...the contents of the register...being compared with the contents of the counter associated to the height* ***(each transponder includes a counter for counting interrogate pulses and a decoding circuit (emphasis) which initiates generation of a reply pulse when the interrogate pulse count is equal to a number assigned to one of its transducers; Column 5, lines 46-55)***," the combination of Turner et al., Olarig, and Sotek et al. does not disclose methods and components relating to height, which Comiskey et al. discloses **[x, y, and z (with z being analogous to height) pixels are present, resulting in a three-dimensional addressing scheme (Page 3, paragraph 0049)]**.

Turner et al., Olarig, Sotek et al., and Comiskey et al. are analogous art in that they both focus on addressing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by the combination of Turner et al., Olarig, and Sotek et al. to also include coordinates and supporting components for height as disclosed by Comiskey et al.

The motivation for doing so is substituting a three-dimensional addressing scheme for a two-dimensional one can help reduce the number of drivers needed to run each pixel **[Page 3, paragraph 0049]**, with the problem concerning the sheer number of

drivers required being disclosed on **[Page 2, paragraph 0011]**. Since Comiskey et al. calls the addressing system "*three-dimensional addressing*," it would immediately be obvious to one skilled in the art that such a system can also apply to addressing units/pixels in three dimensions.

As per **claim 24**, the combination of Turner et al., Olarig, Sotek et al., and Comiskey et al. discloses "*the method*" (*see rejection to* ***claim 23*** *above*). Comiskey et al. further discloses the idea where the height value is affected while the line and column values are reset in "*the control circuit transmits height increment signals causing the additional counters associated to the height to be incremented and the line and column counters of all the microsystems to be reset* ***(the system has the plurality of pixels arranged in sub-arrays containing the first and second sets of addressing means, with the sub-arrays being denoted by the third set of addressing means. Depending on the value of the third set of addressing means, the first and second sets of addressing means are not utilized or ignored; Page 3-4, paragraph 0050)***."

CLOSING COMMENTS

7. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENRY YU whose telephone number is (571)272-9779. The examiner can normally be reached on Monday to Friday, 8:00 AM to 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TARIQ HAFIZ can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. Y./
Examiner, Art Unit 2182
December 9, 2009

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182